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(54) **INTEGRATED CHIP PACKAGE STRUCTURE USING SILICON SUBSTRATE AND METHOD OF MANUFACTURING THE SAME**

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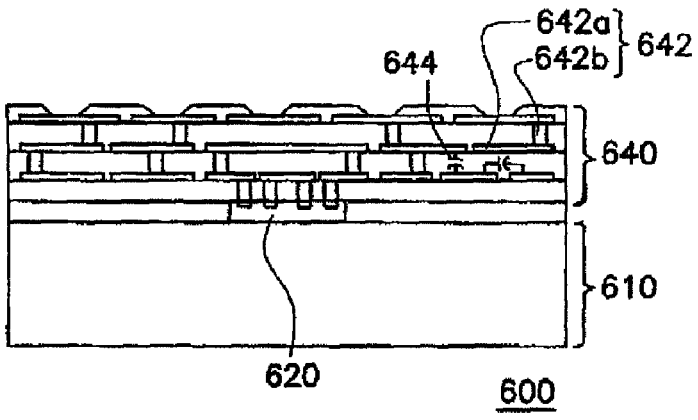
(57) **ABSTRACT**

An integrated chip package structure and method of manufacturing the same is by adhering dies on a silicon substrate and forming a thin-film circuit layer on top of the dies and the silicon substrate. Wherein the thin-film circuit layer has an external circuitry, which is electrically connected to the metal pads of the dies, that extends to a region outside the active surface of the dies for fanning out the metal pads of the dies. Furthermore, a plurality of active devices and an internal circuitry is located on the active surface of the dies. Signal for the active devices are transmitted through the internal circuitry to the external circuitry and from the external circuitry through the internal circuitry back to other active devices. Moreover, the chip package structure allows multiple dies with different functions to be packaged into an integrated package and electrically connecting the dies by the external circuitry.

42 Claims, 16 Drawing Sheets



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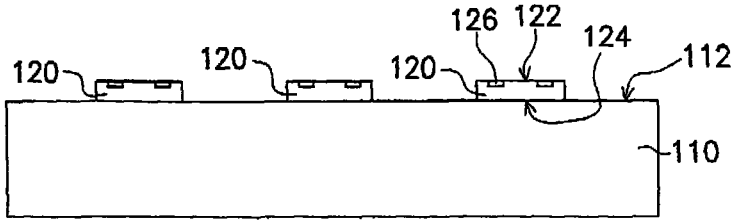
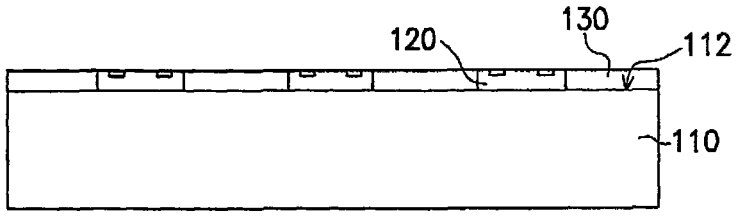


FIG. 1A



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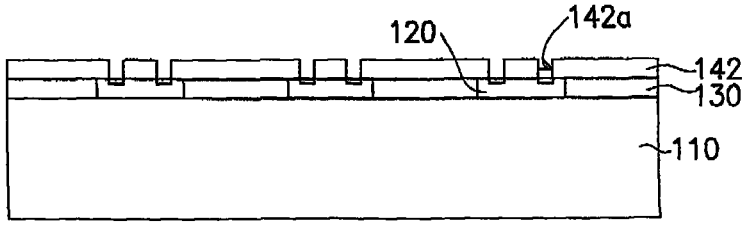

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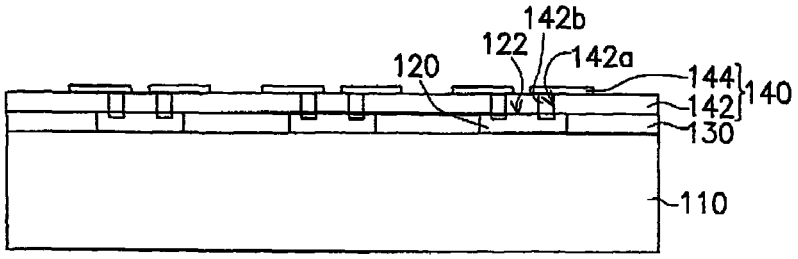


FIG. 1D

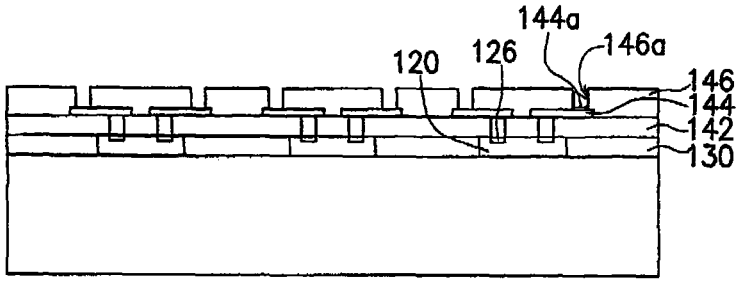
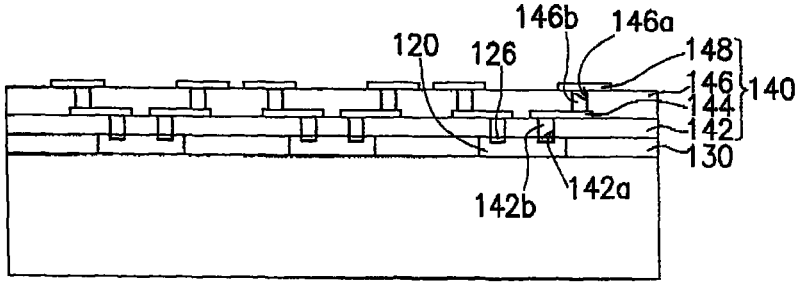


FIG. 1E



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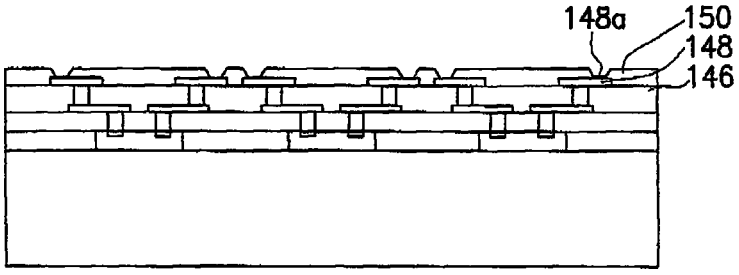


FIG. 1G

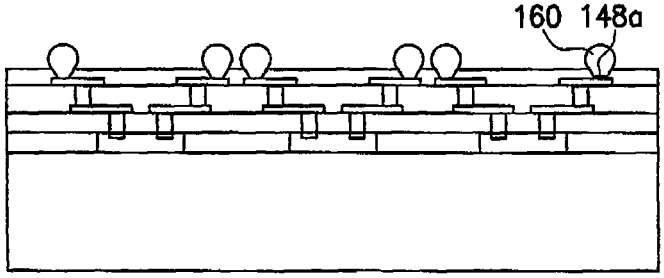


FIG. 1H

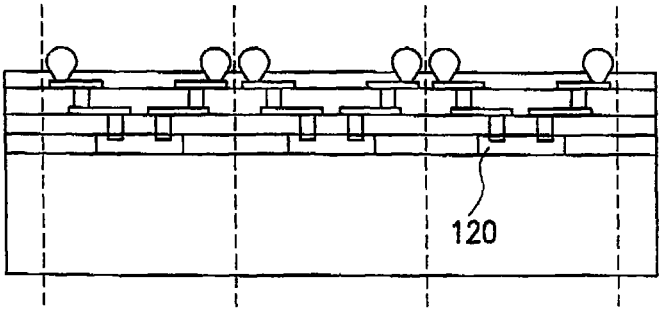


FIG. 1I

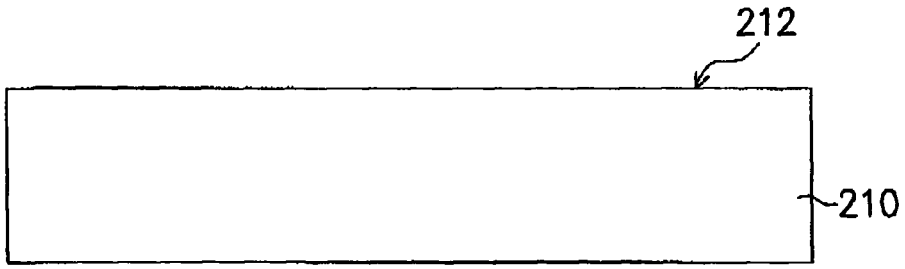
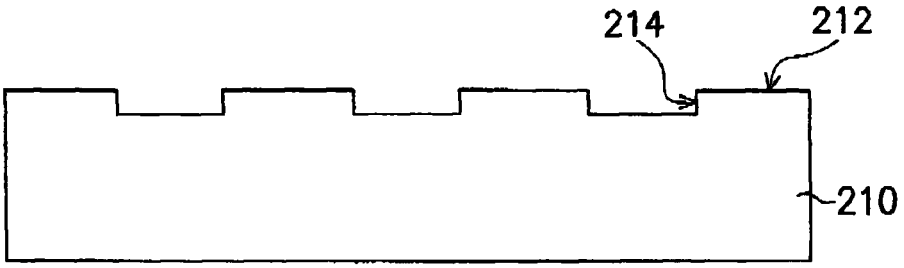


FIG. 2A



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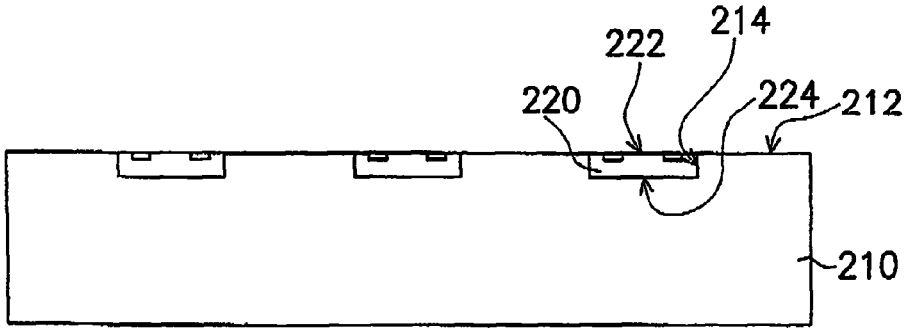

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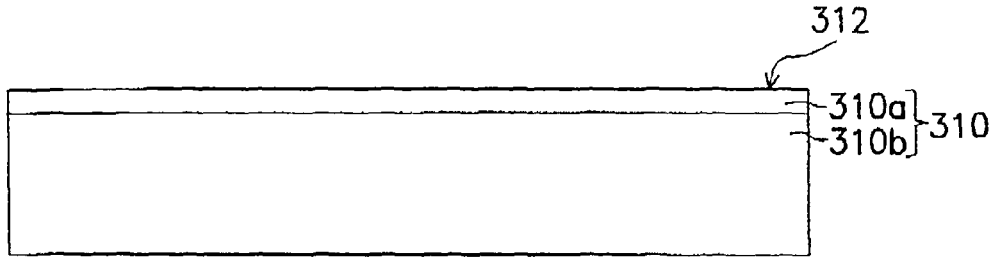
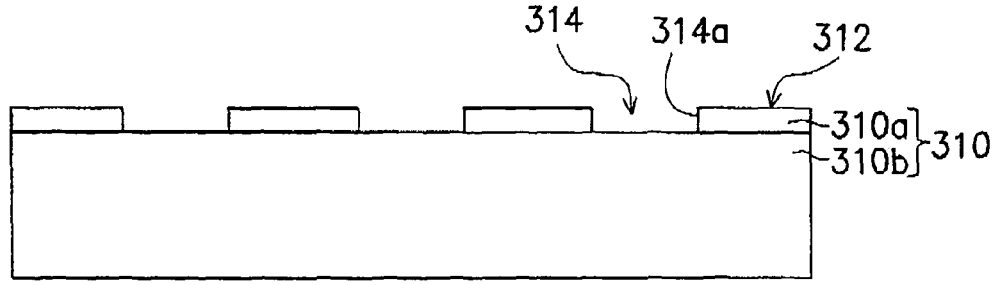


FIG. 3A



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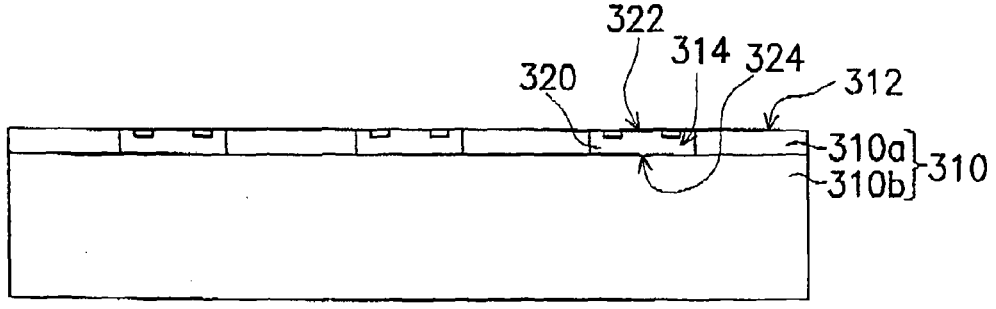

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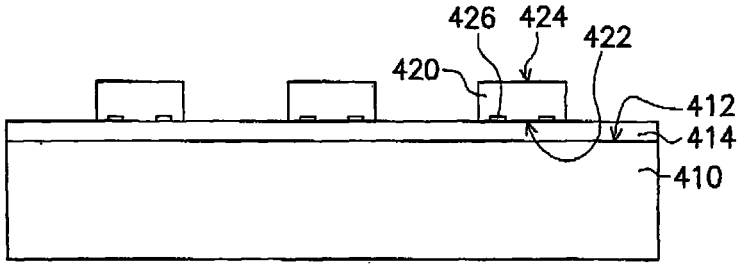
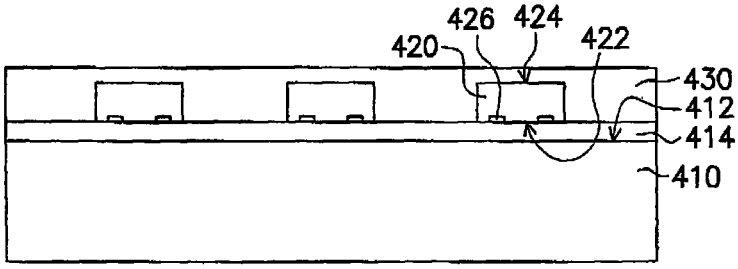


FIG. 4A



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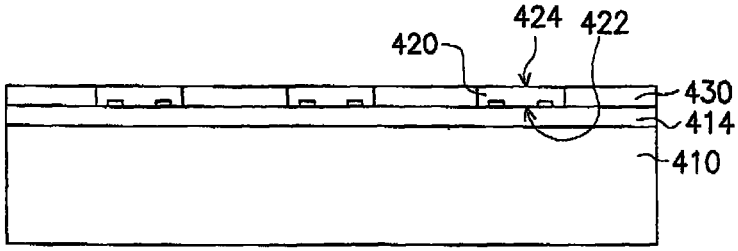

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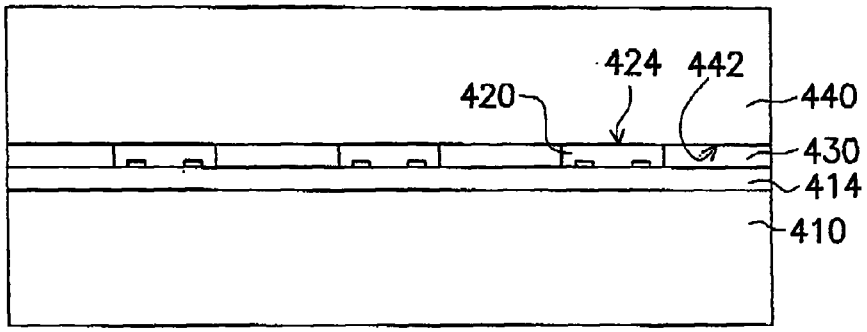

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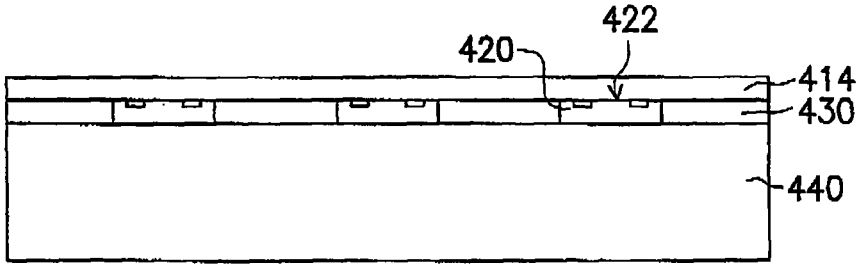

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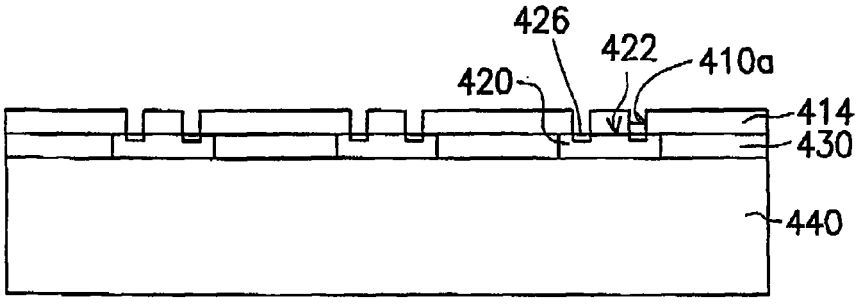

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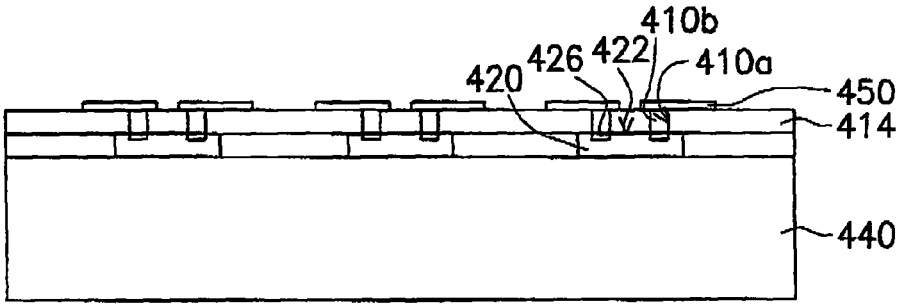


FIG. 4G

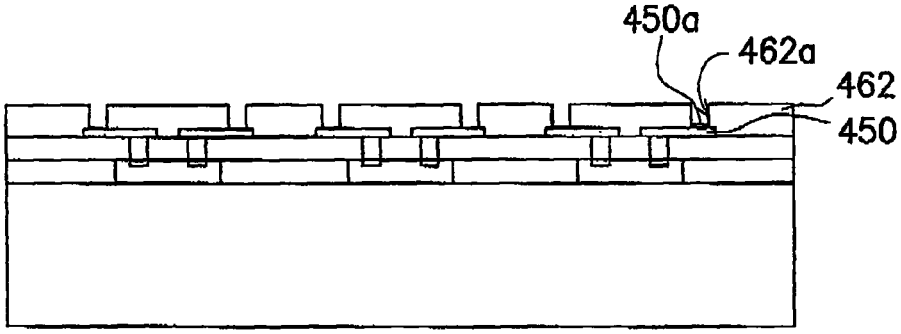


FIG. 4H

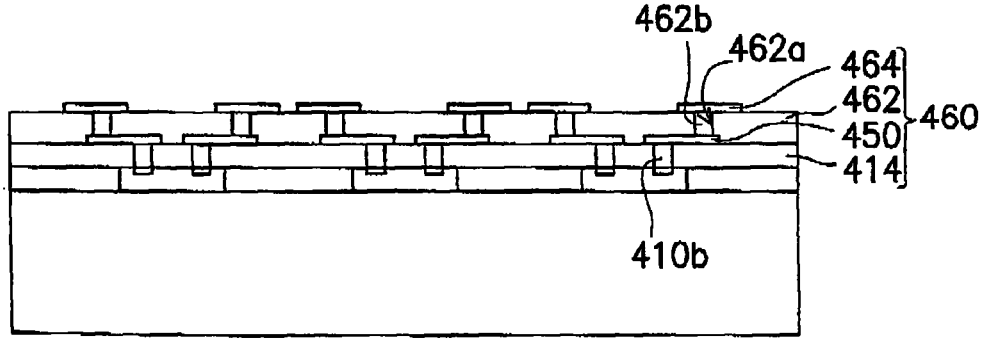


FIG. 4I

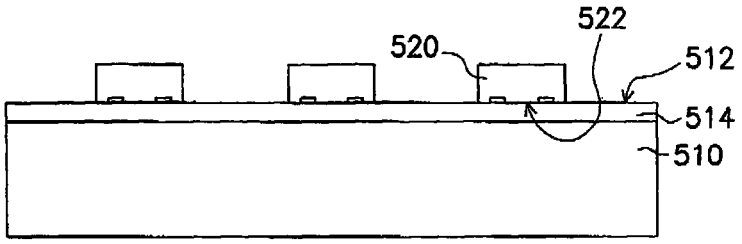
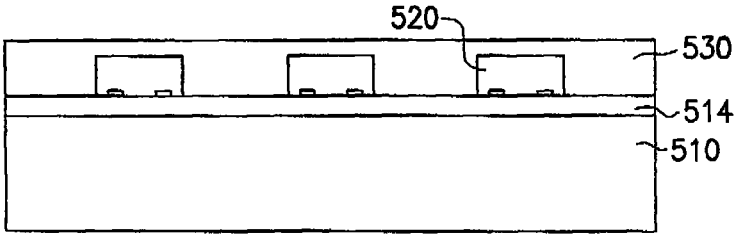


FIG. 5A



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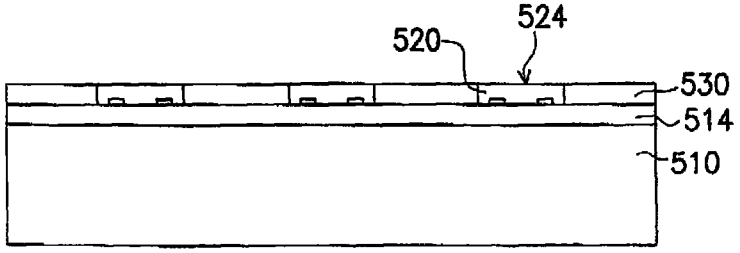

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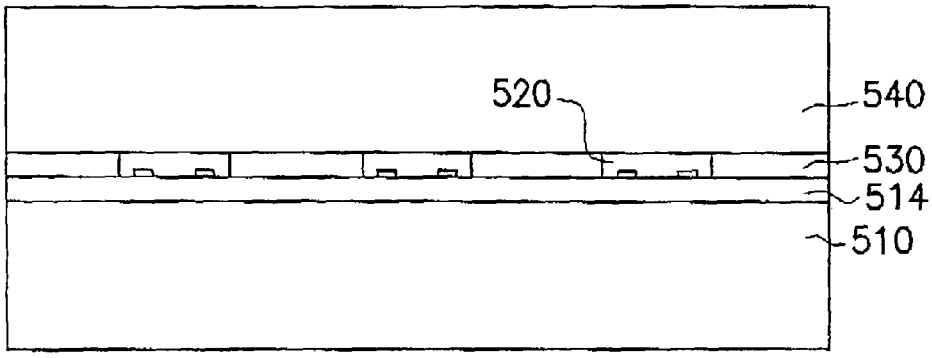


FIG. 5D

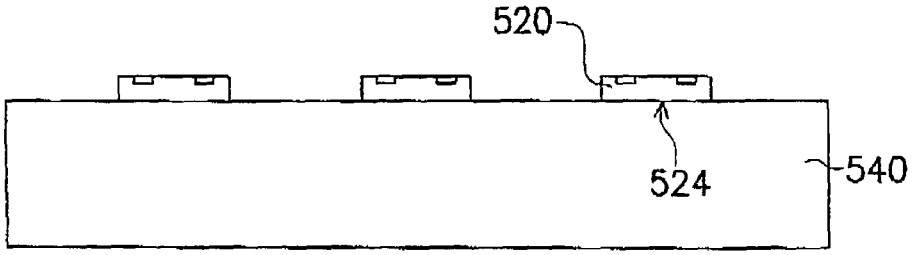
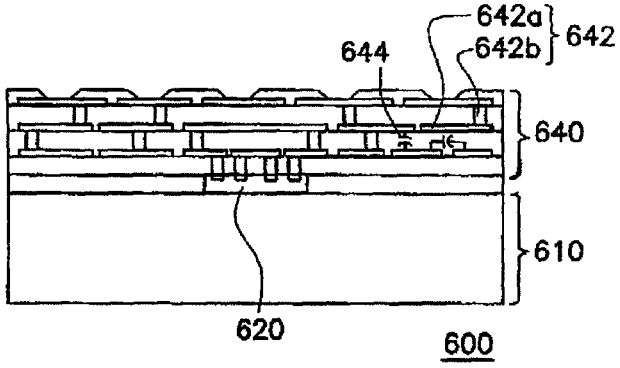


FIG. 5E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600

FIG. 6

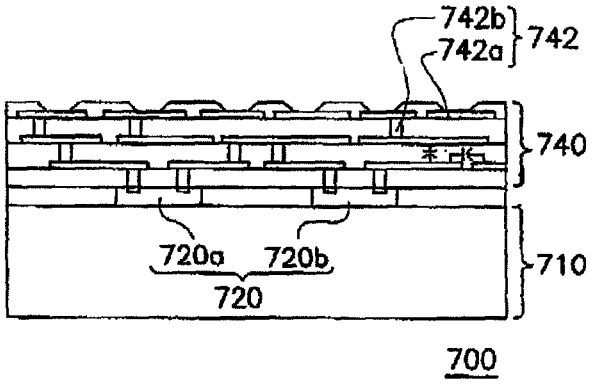
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FIG. 7

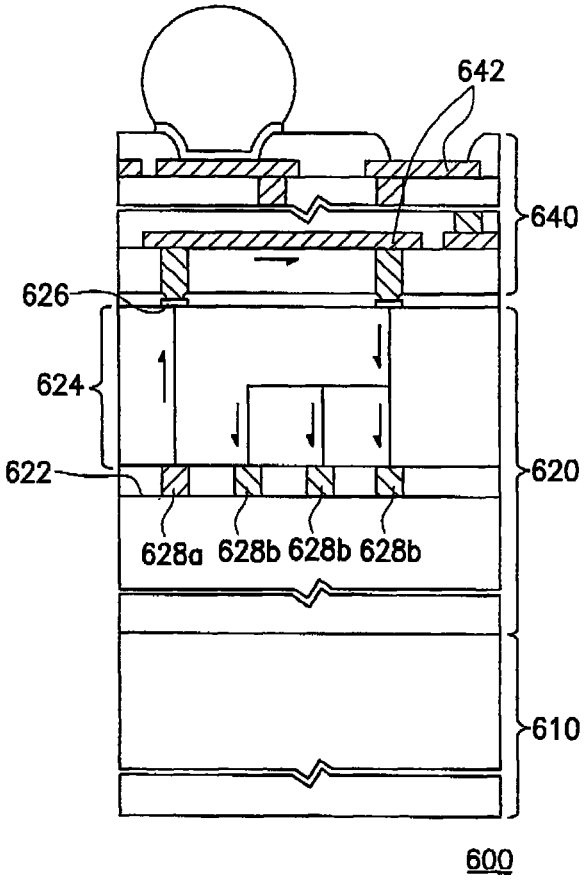

FIG. 8

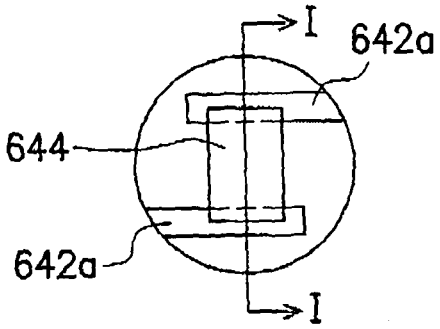

FIG. 9A

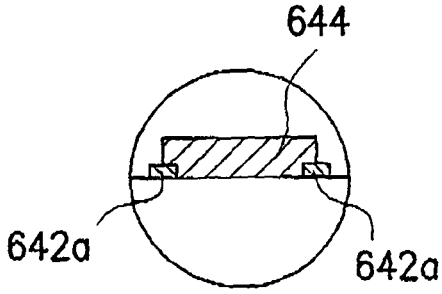

FIG. 9B

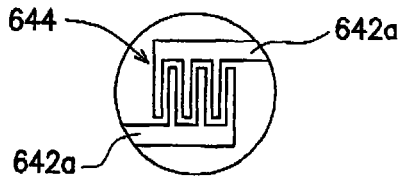

FIG. 10A

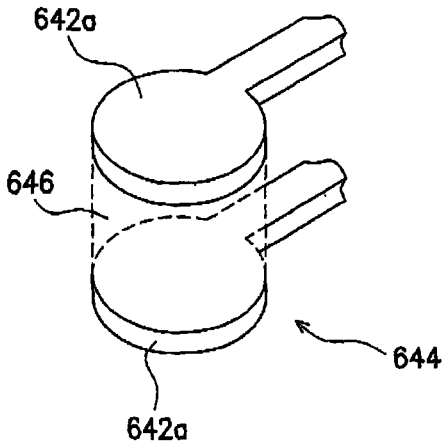

FIG. 10B

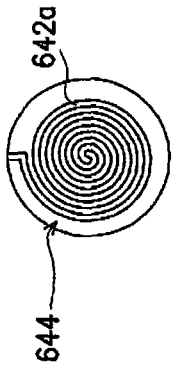

FIG. 11A

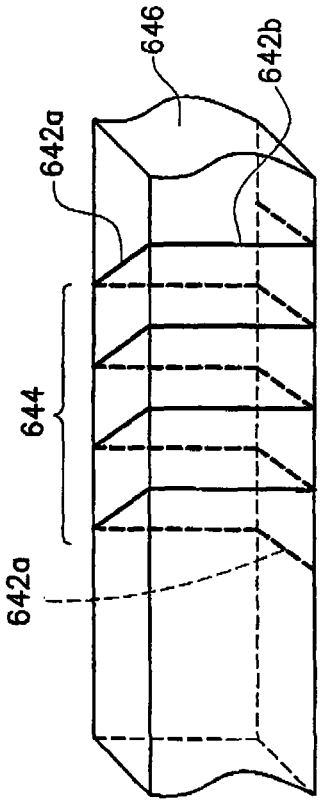

FIG. 11B

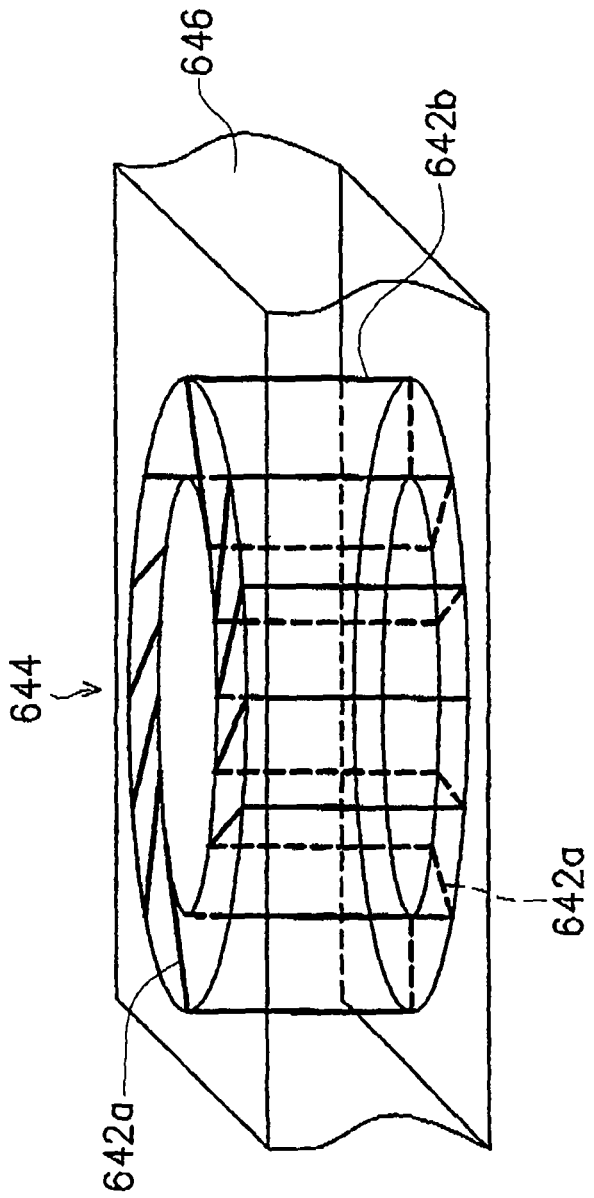

FIG. 11C

INTEGRATED CHIP PACKAGE STRUCTURE USING SILICON SUBSTRATE AND METHOD OF MANUFACTURING THE SAME

This application is a divisional application of, and claims the priority benefit of, U.S. application Ser. No. 10/055,568 filed on Jan. 22, 2002.

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90133195, filed Dec. 31, 2001.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an integrated chip package structure and method of manufacture the same. More particularly, the present invention relates to an integrated chip package structure and method of manufacture the same using silicon substrate.

2. Description of Related Art

In the recent years, the development of advanced technology is on the cutting edge. As a result, high-technology electronics manufacturing industries launch more feature-packed and humanized electronic products. These new products that hit the showroom are lighter, thinner, and smaller in design. In the manufacturing of these electronic products, the key device has to be the integrated circuit (IC) chip inside any electronic product.

The operability, performance, and life of an IC chip are greatly affected by its circuit design, wafer manufacturing, and chip packaging. For this present invention, the focus will be on chip packaging technique. Since the features and speed of IC chips are increasing rapidly, the need for increasing the conductivity of the circuitry is necessary so that the signal delay and attenuation of the dies to the external circuitry are reduced. A chip package that allows good thermal dissipation and protection of the IC chips with a small overall dimension of the package is also necessary for higher performance chips. These are the goals to be achieved in chip packaging.

There are a vast variety of existing chip package techniques such as ball grid array (BGA), wire bonding, flip chip, etc. . . for mounting a die on a substrate via the bonding points on both the die and the substrate. The inner traces helps to fan out the bonding points on the bottom of the substrate. The solder balls are separately planted on the bonding points for acting as an interface for the die to electrically connect to the external circuitry. Similarly, pin grid array (PGA) is very much like BGA, which replaces the balls with pins on the substrate and PGA also acts an interface for the die to electrically connect to the external circuitry.

Both BGA and PGA packages require wiring or flip chip for mounting the die on the substrate. The inner traces in the substrate fan out the bonding points on the substrate and electrical connection to the external circuitry is carried out by the solder balls or pins on the bonding points. As a result, this method fails to reduce the distance of the signal transmission path but in fact increase the signal path distance. This will increase signal delay and attenuation and decrease the performance of the chip.

Wafer level chip scale package (WLCSP) has an advantage of being able to print the redistribution circuit directly on the die by using the peripheral area of the die as the bonding points. It is achieved by redistributing an area array on the surface of the die, which can fully utilize the entire area of the die. The bonding points are located on the redistribution circuit by forming flip chip bumps so the bottom side of the die connects directly to the printed circuit board (PCB) with micro-spaced bonding points.

Although WLCSP can greatly reduce the signal path distance, it is still very difficult to accommodate all the bonding points on the die surface as the integration of die and internal devices gets higher. The pin count on the die increases as integration gets higher so the redistribution of pins in an area array is difficult to achieve. Even if the redistribution of pins is successful, the distance between pins will be too small to meet the pitch of a printed circuit board (PCB).

SUMMARY OF THE INVENTION

Therefore the present invention provides an integrated chip package structure and method of manufacturing the same that uses the original bonding points of the die and connect them to an external circuitry of a thin-film circuit layer to achieve redistribution. The spacing between the redistributed bonding points matches the pitch of aPCB.

In order to achieve the above object, the present invention presents a chip package structure and method of manufacturing the same by adhering the backside of a die to a silicon substrate, wherein the active surface of the die has a plurality of metal pads. A thin-film circuit layer is formed on top of the die and the silicon substrate, where the thin-film circuit layer has an external circuitry that is electrically connected to the metal pads of the die. The external circuitry extends to a region that is outside the active area of the dies and has a plurality of bonding pads located on the surface layer of the thin-film layer circuit. The active surface of the die has an internal circuitry and a plurality of active devices, where signals can be transmitted from one active device to the external circuitry via the internal circuitry, then from the external circuitry back to another active device via the internal circuitry. Furthermore, the silicon substrate has at least one inwardly protruded area so the backside of the die can be adhered inside the inwardly protruded area and exposing the active surface of the die. Wherein the silicon substrate is composed of a silicon layer and a heat insulating material formed overlapping and the inwardly protruded areas are formed by overlapping the silicon substrate with openings on the heat conducting layer. Futhermore, the present chip package structure allows multiple dies with same or different functions to be packaged into one integrated chip package and permits electrically connection between the dies by the external circuitry.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTIOIN OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

FIGS. **1**A to **1**I are schematic diagrams showing the sectional view of the structure of the first embodiment of the present invention.

FIGS. **2**A to **2**C are schematic diagrams showing the sectional view of the structure of the second embodiment of the present invention.

FIGS. **3**A to **3**C are schematic diagrams showing the sectional view of the structure of the third embodiment of the present invention.

FIGS. **4**A to **4**I are schematic diagrams showing the sectional view of the structure of the forth embodiment of the present invention.

FIGS. **5**A to **5**E are schematic diagrams showing the sectional view of the structure of the fifth embodiment of the present invention.

FIG. **6** is a schematic diagram showing the sectional view of the chip package structure of a preferred embodiment of the present invention with one die.

FIG. **7** is a schematic diagram showing the sectional view of the chip package structure of a preferred embodiment of the present invention with a plurality of dies.

FIG. **8** is a magnified diagram showing the sectional view of the chip package structure of a preferred embodiment of the present invention.

FIGS. **9**A, **9**B are schematic diagrams of the top and side view respectively of the patterned wiring layer of the thin-film circuit layer with a passive device.

FIG. **10**A is a schematic diagram of the formation of a passive device by a single layer of patterned wiring layer of the thin-film circuit layer.

FIG. **10**B is a schematic diagram of the formation of a passive device by a double layer of patterned wiring layer of the thin-film circuit layer.

FIG. **11**A is a schematic diagram of the formation of a passive device by a single layer of patterned wiring layer of the thin-film circuit layer.

FIG. **11**B is a schematic diagram of the formation of a passive device by a double layer of patterned wiring layer of the thin-film circuit layer.

FIG. **11**C is a schematic diagram of the formation of a passive device by a double layer of patterned wiring layer of the thin-film circuit layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Please refer to FIG. **1**A, a silicon substrate **110** with a surface **112** and a plurality of dies **120** are provided. Dies **120** have an active surface **122** and a backside **124** is also provided, where the active devices are formed on active surface **122** of the dies. Furthermore, dies **120** have a plurality of metal pads **126** located on active surface **122** of dies **120** acting as the output terminal of dies **120** to transmit signals to the external circuitry. Backside **124** of dies **120** is adhered to surface **112** of silicon substrate **110** by a conductive paste or adhesive tape. Therefore, active surface **122** of dies **120** is facing upwards along surface **112** of silicon substrate **110**.

Please refer to FIG. **1**B, when adhering die **120** to silicon substrate **110**, a filling layer **130** can be formed on top of surface **112** of silicon substrate **100** surrounding the peripheral of dies **120** to fill the gap between dies **120**. The height of filling layer **130** should be approximately equal to the height of active surface **122** of dies **120**. The material of filling layer **130** can be epoxy, polymer, or the like. After curing of filling layer **130**, a grinding or etching process is applied to planarize filling layer **130** so the top face of filling layer **130** is planar with active surface **122** of dies **120**.

Please refer to FIG. **1**C, after the formation of filling layer **130** on silicon substrate **110**, a dielectric layer **142** is deposited on top of filling layer **130** and active surface **122** of dies **120**. Dielectric layer **142** is patterned according to metal pads **126** on dies **120** to form thru-holes **142***a*. The material of dielectric layer **142** can be poly-Imide (PI), benzocyclobutene (BCB), porous dielectric material, stress buffer material, or the like. Patternization of dielectric layer **142** can be performed by photo via, laser ablation, plasma etching, or the like.

Please continue to refer to FIG. **1**C, filling layer **130** is used to support dielectric layer **142** so dielectric layer **142** can be formed planarized on top of silicon substrate **110** and dies **120** without an uneven surface. As a result, after dielectric layer **142** is formed on surface **112** of silicon substrate **110** and active surface **122** of dies **120**, dielectric layer **142** also fills the peripheral of dies **120**, meaning the gap between dies **120**. Therefore the bottom structure of dielectric layer **142** can replace the structure of filling layer **130** covering entirely surface **112** of silicon substrate **110** and surrounding dies **120**. The method of forming dielectric layer **142** includes first depositing a layer of dielectric layer **142** entirely over dies **120** and silicon substrate **110**, then after curing, a grinding or etching process is performed to planarize dielectric layer **142**.

Please refer to FIG. **1**D, after forming dielectric layer **142** and patterning dielectric layer **142** to form thru-holes **142***a*, a patterned wiring layer **144** is formed by photolithography and sputtering, electroplating, or electro-less plating. Wherein part of the conductive material from patterned wiring layer **144** will be injected into thru-holes **142***a* to form vias **142***b*, copper (Cu) is used as the material for patterned wiring layer **144**. Moreover, thru-holes **142***a* can be pre-filled with a conductive material such as a conductive glue to form vias **142***b*. Therefore no matter if the thru-holes are filled with the conductive material from patterned wiring layer **144** or pre-filled with a conductive material, patterned wiring layer **144** is electrically connected to metal pads **126** of dies **120**. It is to be noted that part of patterned wiring layer **144** extends to a region outside active surface **122** of dies **120**. Dielectric layer **142** and patterned wiring layer **144** form a thin-film circuit layer **140**.

Please refer to FIG. **1**E, after the formation of patterned wiring layer **144**, another dielectric layer **146** can be formed similarly to dielectric layer **142** on top of dielectric layer **142** and patterned wiring layer **144**. Dielectric layer **146** is also patterned to form thru-holes **146***a*, whereas thru-holes **146***a* correspond to bonding pads **144***a* of patterned wiring layer **144**.

Please refer to FIG. **1**F, after the formation and patternization of dielectric layer **146** to form thru-holes **146***a*, a patterned wiring layer **148** can be formed on dielectric layer **146** in a similar way as patterned wiring layer **144**. Wherein part of the conductive material from patterned wiring layer **148** will be injected into thru-hole **146***a* forming a via **146***b*. By the same token, patterned wiring layer **148** is electrically connected to patterned wiring layer **144** by vias **146***b*, and further electrically connected to metal pads **126** of die **120** by vias **142***b* of thru-hole **142***a*. Therefore, thin-film circuit layer **140** further comprises dielectric layer **146**, a plurality of vias **146***b*, and patterned wiring layer **148**.

Please continue to refer to FIG. **1**F, in order to redistribute all metal pads **126** of dies **120** on silicon substrate **110**, the number of patterned wiring layers (**144**, **148** . . .) and dielectric layers (**142**, **146** . . .) for electrical insulation may be increased. All patterned wiring layers (**144**, **148** . . .) are electrically connected by vias (**146***b* . . .) of thru-holes (**146***a* . . .). However if only the first patterned wiring layer **144** is required to entirely redistribute metal pads **126** of dies **120** on silicon substrate **110**, extra dielectric layers (**146** . . .) and patterned wiring layers (**148** . . .) will no longer be required in the structure. In other words, thin-film circuit layer **140** comprises at least one dielectric layer **142**, one patterned wiring layer **144**, and a plurality of vias **142***b*.

Wherein patterned wiring layer (**144**, **148** . . .) and vias (**142***b*, **146***b* . . .) of thin-film circuit layer **140** form an external circuitry of thin-film circuit layer **140**.

Please refer to FIG. **1**G, after the formation of patterned wiring layer **148**, a patterned passivation layer **150** is formed on top of dielectric layer **146** and patterned wiring layer **148**. Patterned passivation layer **150** is used to protect patterned wiring layer **148** and expose the plurality of bonding pads **148***a* of patterned wiring layer **148**, whereas some of bonding pads **148***a* are in a region outside of active surface **122** of dies **120**. As previously mentioned, the redistribution of metal pads **126** on silicon substrate **110** requires multiple layers of patterned wiring layers (**144**, **148** . . .) and a patterned passivation layer **150** formed on the very top, which is furthest away from silicon substrate **110**. However, if only patterned wiring layer **144** is required to redistribute metal pads **126** of dies **120** on silicon substrate **110**, patterned passivation layer **150** will be formed directly on patterned wiring layer **144**. The material of passivation layer **150** can be anti-solder insulating coating or other insulating material.

Please refer to FIG. **1**H, after the formation of patterned passivation layer **150**, a bonding point **160** can be placed on bonding pads **148***a* serving as an interface for electrically connecting die **120** to the external circuitry. Wherein bonding point **160** illustrated in FIG. **1**H is a ball but it is not limited to any formation, which might include a bump, pin, or the like. Ball connector maybe solder ball, and bump connector maybe solder bump, gold bump, or the like.

Please refer to FIG. **1**I, after the formation of bonding points **160** on bonding pads **148***a*, a singularization process of packaged die **120** by mechanical or laser cutting is performed along the dotted line as indicated in the diagram. Afterwards, the chip package structure of the die is completed.

According to the above, the first embodiment of the present invention is a chip package structure with a silicon substrate and a plurality of dies on it. The external circuitry of the thin-film circuit layer allows the metal pads of the die to fan out. By forming bonding pads corresponding to the metal pads of the dies such as solders balls, bumps, or pins as the signal input terminals, the distance of the signal path is effectively decreased. As a result, signal delay and attenuation is reduced to increase performance of the die.

Furthermore, the fabrication process of semi-conductor includes forming active devices and internal circuitry on the surface of a silicon wafer and singularizing the wafer for individual chips. Therefore the main substance in a chip is silicon. The present invention provides a silicon substrate as the chip package structure to package the chip after adhesion to the silicon substrate. The coefficient of thermal expansion (CTE) of the chip and the silicon substrate is identical which can reduce thermal stress between the chips and the silicon substrate at high operating temperature of the chips. As a result, the life span and durability of the chips after packaging is increased because the metal traces of the chip and silicon substrate will not be stretched.

The second embodiment of the present invention differs from the first embodiment by having inwardly protruded areas in the silicon substrate. This area is for placement of the die with the backside of the die adhered against the bottom of the area so the overall thickness of the chip package structure is reduced. FIGS. **2**A to **2**C are schematic diagrams of the sectional view of the second embodiment illustrating the fabrication of the structure.

Please refer to FIG. **2**A, a silicon substrate **210** with a surface **212** is provided. In FIG. **2**B, multiple inwardly protruded areas **214** on surface **212** of silicon substrate **210** are formed by removing part of silicon substrate **210**. The method of forming inwardly protruded areas **214** includes wet etching at a controlled rate so the depth of each inwardly protruded area **214** is approximately equal to that of die **220**. Therefore the outline and depth of inwardly protruded areas **214** will be the same as dies **220** in FIG. **2**C. The rate of etching can be increased by using KOH, which has a higher corrosiveness on silicon, to improve the speed of the fabrication process. Alternatively, the inwardly protruded areas **214** on silicon substrate **210** can be formed by machining such as milling. In FIG. **2**C, backside **224** of dies **220** is adhered to the bottom of inwardly protruded areas **214** so dies **220** are inlayed in inwardly protruded areas **214**. Active surface **222** of die **220** is exposed along surface **212** or silicon substrate **210**.

The structure of the second embodiment of the present invention after FIG. **2**C will follow FIGS. **1**C to **1**I from the first embodiment of the present invention, therefore it will not be repeated.

The second embodiment of the present invention is a silicon substrate with a plurality of inwardly protruded areas for inlaying dies by adhering the backside of the dies to the bottom of the inwardly protruded areas and exposing the active surface of the dies. A thin-film circuit layer is formed on top of the dies and the silicon substrate to fan out the metal pads of the dies by using the external circuitry of the thin-film circuit layer. Due to the inlay of the dies in the silicon substrate, thinning of the thickness of the chip package structure is effectively achieved and the surface of the silicon substrate provides enough planarity and support for the formation of the thin-film circuit layer.

The third embodiment of the present invention differs from the second embodiment of the present invention by using an integrated silicon substrate with at least one silicon layer and one heat conducting layer. FIGS. **3**A to **3**C are schematic diagrams of the sectional view of the third embodiment illustrating the fabrication of the structure.

Please refer to FIG. **3**A, an integrated silicon substrate **310** consists of a silicon layer **310***a* with multiple openings **314***a* and a heat conducting layer **310***b*, wherein the material of heat conducting layer **310***b* maybe metal. In FIG. **3**B, part of silicon layer **310***a* is removed and placed overlapping heat conducting layer **310***b* so openings **314***a* of silicon layer **310***a* form inwardly protruded areas **314**, wherein silicon layer **310***a* is wet etched downwards until reaching the surface of heat conducting layer **310***b*. Following in FIG. **3**C, backside **324** of die **320** is adhered to the bottom of inwardly protruded areas **314** so dies **320** are inlayed in silicon substrate **310** with active surface **322** of die **320** exposed along surface **312** of silicon substrate **310**.

The structure of the third embodiment of the present invention after FIG. **3**C will follow FIGS. **1**C to **1**I from the first embodiment of the present invention, therefore it will not be repeated.

The third embodiment of the present invention is an integrated silicon substrate with a silicon layer with a plurality of openings and a heat conducting layer, wherein the openings are formed by etching. The openings on the silicon layer will form inwardly protruded areas on the integrated silicon substrate. The backside of the die adheres to the bottom of the inwardly protruded areas so the dies are inlayed in the inwardly protruded areas exposing the active surface of the dies.

As mentioned above, this integrated silicon substrate can efficiently dissipate heat from the dies to the outside because the bottom of the inwardly protruded area is the surface of the heat conducting material. The surface of the silicon substrate provides enough planarity and support for the formation of the thin-film circuit layer. Moreover, the CTE of the chips and

substrate is identical so thermal stress between the chips and the silicon substrate is greatly reduced because the metal traces on the chips are not stretched to increase the life span and durability of the chips.

The fourth embodiment of the present invention is slightly different from the first three embodiments. FIGS. **4**A to **4**E are schematic diagrams of the sectional view of the fourth embodiment illustrating the fabrication of the structure.

Please refer to FIG. **4**A, a silicon substrate **410** with a first surface **412** and an insulating layer **414** of material such as metal nitride or metal oxide formed on top of first surface **412** of silicon substrate **410**. The thickness of insulating layer **414** is about 2 microns to 200 microns, usually 20 microns. Following, a plurality of dies **420** having an active surface **422**, a backside **424**, and a plurality of metal pads **426** located on active surface **422** is provided. The fourth embodiment of the present invention differs from the third embodiment of the present invention by placing active surface **422** of die **420** downwards facing first surface **412** of silicon substrate **410**.

Please refer to FIG. **4**B, a filling layer **430** is formed on top of insulating layer **414** after active surface **422** of die **420** is adhered to first surface **412** of silicon substrate **410**. Filling layer **430** covers entirely first surface **412** of silicon substrate **410** and surrounds dies **420**. The material of filling layer **430** maybe an oxide, epoxy, or the like.

Please refer to FIG. **4**C, after the formation of filling layer **430**, a planarization process such as chemical mechanical polishing (CMP) is performed to planarize filling layer **430** and backside of die **420**. Although the thickness of the active devices and wiring (not shown) on active surface **422** of die **420** is much less than that of die **420**, the thickness of die **420** should not be too small because cracks or damage to the die will occur during machine handling (for example vacuum suction). However the present invention directly adheres active surface **422** of die **420** on first surface **412** of silicon substrate **410** without further machine handling. Afterwards a CMP process is performed on backside **424** of dies **420** to reduce the thickness of dies **420**. As a result, dies **420** are ground to a very small thickness allowing the final chip package structure to be much thinner.

Please refer to FIG. **4**D, after the planarization of filling layer **430** and dies **420**, a second silicon substrate **440** with a second surface **442** is adhered to filling layer **430** and dies **420** creating a sandwich effect with filling layer **430** and dies **420** in between two silicon substrates **410** and **440**.

Please refer to FIG. **4**E, after the adhesion of second silicon substrate **440**, first silicon substrate **410** is removed by etching until reaching insulating **414** and preserving insulating layer **414** on top of dies **410** and filling layer **430**. First silicon substrate is used to provide a planar surface (surface **412** in FIG. **4**A) for the adhesion and formation of insulating layer **414**. Therefore first silicon substrate can be replaced by substrate of other material such as glass, ceramic, metal, or other organic material.

Please refer to FIG. **4**F, after the thinning of first silicon substrate **410**, a plurality of first thru-holes **410***a* are formed on insulating layer **414** for exposing metal pads **426** of active surface **422** of die **420**. First thru-holes **410***a* can be formed by machine drilling, laser, plasma etching, or similar methods.

Please refer to FIG. **4**G, a first patterned wiring layer **450** is formed on insulating layer **414**. Using the same method disclosed in the first embodiment of the present invention, first vias **410***b* in first thru-holes **410***a* are formed by either filling first thru-holes **410***a* with part of the conductive material from patterned wiring layer **450** or pre-filling first thru-holes **410***a* with a conductive material before the formation of patterned wiring layer **450**. A part of patterned wiring layer **450** will extend to a region outside active surface **422** of die **420**.

Please refer to FIG. **4**H, a dielectric layer **462** is formed on insulating layer **414** and first patterned wiring layer **450**. Wherein dielectric layer **462** is patterned to form a plurality of second thru-holes **462***a*, which correspond to bonding pad **450***a* of patterned wiring layer **450**.

Please refer to FIG. **4**I, a second patterned wiring layer **464** is formed on dielectric layer **462**. Using the same method as above, second vias **462***b* in second thru-holes **462***a* can be formed by either filling second thru-holes **462***a* with part of the conductive material from patterned wiring layer or pre-fill second thru-holes **462***a* with a conductive material before the formation of patterned wiring layer **464**. Similarly, in order to redistribute metal pads **426** of dies **420** on second silicon substrate **440**, dielectric layer (**462** . . .), second vias (**462***a* . . .), and second patterned wiring layer (**464** . . .) can be repeatedly formed on dies **420** and silicon substrate **440**. Wherein insulating layer **414**, first patterned wiring layer **450**, dielectric layer **462** . . . , and second patterned wiring layer **464** . . . form thin-film circuit layer **460**. First vias **410***b*, first patterned wiring layer **450**, second vias **462***b* . . . , and second patterned wiring layer **464** form the external circuitry of thin-film circuit layer **460**.

The structure of the fourth embodiment of the present invention after FIG. **4**I will follow FIGS. **1**G to **1**I from the first embodiment of the present invention, therefore it will not be repeated.

The fourth embodiment of the present invention is a silicon substrate with the active surface of the dies directly adhered to the insulating layer of the first silicon substrate. A filling layer is formed over the dies and the silicon substrate followed by a planarization and thinning process. Afterwards, a second silicon substrate is adhered to the die and the filling layer. A plurality of thru-holes filled with conductive material are formed on the insulating layer. Finally, a patterned wiring layer is formed on the insulating layer allowing the external circuitry of the thin-film circuit layer to extend to a region outside the active surface of the die to help fan out the metal pads of the die.

The advantage of this structure is increased surface stability and accuracy because the active surface of the dies are first adhered to the surface of the first silicon substrate. The thickness of the die can be very small for reducing the overall thickness of the chip package because no machines handling of dies is required.

The fifth embodiment of the present invention takes the first half of the fabrication process from the fourth embodiment of the present invention and combines with the second half of the fabrication process from the first embodiment of the present invention. FIGS. **5**A to **5**E are schematic diagrams of the sectional view illustrating the fabrication of the structure.

Please refer to FIG. **5**A, an insulating layer **514** is formed on top of first surface **512** of silicon substrate **510**. Following, an active surface **522** of dies **520** is adhered to a first surface **512** of insulating layer **514**. Wherein the material of insulating **514** includes metal nitride or metal oxide. In FIG. **5**B, a filling layer **530** is formed on top of dies **520** and insulating layer **514** covering dies **520**.

In FIG. **5**C, a planarization and thinning process of dies **520** and filling layer **530** is performed to planarize backside **524** of dies **520** and filling layer **530**. In FIG. **5**D, a second silicon substrate **540** is formed on top of dies **520** and filling layer **530** so backside **524** of dies **520** adheres to second silicon substrate **540**. By removing filling layer **530**, first silicon sub-

strate **510**, and insulating layer **514**, the metal pads on active surface **522** of dies **520** are exposed, as illustrated in FIG. **5**E.

First silicon substrate **510** and is used to supply a planarized surface (first surface **512**), and will be removed in later stages of the fabrication process. Therefore first silicon substrate **510** can be replaced by substrates of other materials such as glass, metal, silicon, metal, or other organic material. Similarly, insulating layer **514** of first silicon substrate is also removed in later stages of the fabrication process. Therefore it is not necessary to form insulating layer **414** on top of first silicon substrate **510** and directly adheres active surface **522** of dies **520** to first surface **512** of first silicon substrate **510**.

The structure of the fifth embodiment of the present invention after FIG. **5**E will follow FIGS. **1**B to **11** of the first embodiment of the present invention, therefore it will not be repeated.

The fifth embodiment of the present invention is a silicon substrate with the active surface of the die adhered to the insulating layer of the first silicon substrate for allowing high surface stability and accuracy. As a result, it eliminates the need of machine handling of the dies to achieve a very small thickness of the die for reducing the overall thickness of the chip package.

Furthermore, please refer to FIG. **6**, it illustrates the schematic diagram of the sectional view of the chip package structure **600** of the present invention for a single die **620**. Die **620** is placed on silicon substrate **610**, and a thin-film circuit layer **640** is formed on top of die **620** and silicon substrate **610**. External circuitry **642** of thin-film circuit layer **640** has at least has one patterned wiring layer **642***a* and a plurality of vias **642***b*. The thickness of the inner traces inside die **620** is usually under 1 micron, but because the high amount of traces collocated together so RC delay is relatively high and the power/ground bus requires a large area. As a result, the area of die **620** is not enough to accommodate the power/ground bus. Therefore the chip package structure **600** uses thin-film circuit layer **640** and external circuitry **642** with wider, thicker, and longer traces to alleviate the problem. These traces act an interface for transmitting signals for the internal circuitry of die **620** or the power/ground bus of die **620**. This will improve the performance of die **620**.

Please refer to FIG. **8**, it illustrates a magnified view of the sectional view of the chip package structure of the present invention. Active surface **622** of die **620** has a plurality of active devices **628***a*, **628***b*, and an internal circuitry **624**. The internal circuitry **624** forms a plurality of metal pads **626** on the surface of die **620**. Therefore signals are transmitted from active devices **628***a* to external circuitry **642** via internal circuitry **624** of die **620**, and from external circuitry **642** back to another active device **628***b* via internal circuitry **624**. The traces of external circuitry **642** are wider, longer, and thicker than that of internal circuitry **624** for providing an improved transmission path.

Please continue to refer to FIG. **6**, external circuitry **642** further comprises at least one passive device **644** including a capacitor, an inductor, a resistor, a wave-guide, a filter, a micro electronic mechanical sensor (MEMS), or the like. Passive device **644** can be located on a single layer of patterned wiring layer **642***a* or between two layers of patterned wiring layers **642***a*. In FIGS. **9**A, **9**B, passive device **644** can be formed by printing or other method on two bonding points on patterned wiring layer **642***a* when forming thin-film layer **640**. In FIG. **10**A, a comb-shape passive device **644** (such as a comb capacitor) is formed directly on a single patterned wiring layer. In FIG. **10**B, passive device **644** (such as a capacitor) is formed between two layers of patterned wiring layers **642***a* with an insulating material **646** in between. Wherein the original dielectric layer (not shown) can replace insulating material **646**. In FIG. **11**A, passive device **644** (such as an inductor) is formed by making a single layer of patterned wiring layer **642***a* into a circular or square (not shown) spiral. In FIG. **11**B, colurrmn-shape passive device **644** (such as an inductor) is formed by using two layers of patterned wiring layers **642***a* and a plurality of vias **642***b* to surround an insulating material **646** forming a column. In FIG. **11**C, circular-shaped passive device **644** (such as an inductor) is formed by using slanted traces from two layers of patterned wiring layers and a plurality of vias **642***b* to surround an insulating material **646** in a circular manner forming a pie. The above structures allow the original externally welded passive devices to be integrated into the inside of the chip package structure.

FIG. **6** illustrates a chip package structure **600** for a single die **620** but FIG. **7** illustrates a chip package structure **700** for a plurality of dies. Chip package structure **700** in FIG. **7** differs from chip package structure **600** in FIG. **6** by having a die module **720**, which comprises at least one or more dies such as die **720***a*, **720***b*. Die **720***a*, **720***b* are electrically connected by the external circuitry of the thin-film circuit layer. The function of die **720***a*, **720***b* can be the same or different and can be integrated together by external circuitry **742** to form a multi-die module (MCM) by packaging same or different dies into one chip package structure. When multiple dies are packaged into the same chip package structure, singulation process is performed on the determined number of dies.

Following the above, the present invention provides a chip packaging method by adhering a die to a silicon substrate or to an inwardly protruded area of a silicon substrate, and forming a thin-film circuit layer with bonding pads and points above the die and silicon substrate. This structure can fan out the metal pads on the die to achieve a thin chip package structure with high pin count.

Comparing to the BGA or PGA package technique used in the prior art, the chip package of the present invention is performed directly on the die and the silicon substrate for fanning out the metal pads on the die. It does not require flip chip or wire bonding to connect the die to the micro-spaced contact points of a package substrate or carrier. The present invention can reduce cost because the package substrate with micro-spaced contacts is very expensive. Moreover the signal transmission path of the present invention is reduced to lessen the effect of signal delay and attenuation, which improves the performance of the die.

Furthermore, the coefficient of thermal expansion (CTE) of the chips and silicon substrate is identical so thermal stress is greatly reduced between the chips and silicon substrate because the expansion between the metal traces on the silicon substrate and the chips is prevented. Consequently, the life span and durability of the chips are increased. Wafer level packaging technique, that is the technique on packaging the chips directly on a chip Wafer, is already well know in the art. Therefore the present invention can adapt currently available chip scale packaging machine to fabricate the silicon substrate using blank silicon chip wafer. As a result the cost fabricating the silicon substrate is greatly reduced and practicality and applicability of the present invention is increased.

Furthermore, the third embodiment of the present invention provides an integrated substrate comprises a silicon layer and a heat conducting layer. A plurality of openings can be pre-formed on the silicon layer by etching so inwardly protruded areas are formed for inlaying the die when the silicon layer overlaps the heat conducting layer. The heat conducting layer helps to dissipate heat to the outside from the die during

operation, which will effectively increase performance. Moreover the CTE of the chips and the silicon substrate is identical so life span and durability of the chips after packaging are increased. The thin-film layer circuit of the present invention is used to transmit signals between two main active devices inside the die, or used as a power/ground bus, or used to add in passive devices. Furthermore, the chip package structure of the present invention can accommodate one or more dies with similar or different functions. The external circuitry of the thin-film circuit layer connects the multiple dies together and can be used in a MCM package. The chip package structure of the present invention adapts the MCM, the external circuitry of the thin-film circuit layer, the passive devices of the external circuitry to form a package that is "system in package".

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A chip package comprising:

a substrate having a surface;

a die-surrounding layer directly on said surface of said substrate;

a die having a backside surface directly on said surface of said substrate, said die disposed between a first portion of said die-surrounding layer and a second portion of said die-surrounding layer, wherein said die has an active surface substantially coplanar with a first surface of said die-surrounding layer, wherein said die comprises a conductive pad within said active surface of said die;

a first dielectric layer on said active surface of said die and said first surface of said die-surrounding layer;

a first patterned conductive layer on said first dielectric layer, on said active surface of said die and on said first surface of said die-surrounding layer, wherein said first patterned conductive layer is coupled to said conductive pad of said die through an opening in said first dielectric layer;

a second dielectric layer on said first patterned conductive layer and on said first dielectric layer;

a second patterned conductive layer on said second dielectric layer, wherein said second patterned conductive layer is coupled to said first patterned conductive layer through an opening in a said second dielectric layer, in which said second patterned conductive layer comprises a portion configured for external coupling of said die; and

a comb-shaped capacitor disposed between said first patterned conductive layer and said second patterned conductive layer.

2. The chip package in claim **1**, wherein said comb-shaped capacitor is aligned with said first portion of said die-surrounding layer.

3. The chip package in claim **1**, wherein said first dielectric layer comprises polyimide.

4. The chip package in claim **1**, wherein said first dielectric layer comprises benzocyclobutene (BCB).

5. The chip package in claim **1**, wherein said first patterned conductive layer comprises electroplated copper.

6. The chip package in claim **1**, wherein said second dielectric layer comprises polyimide.

7. The chip package in claim **1**, wherein said second dielectric layer comprises benzocyclobutene (BCB).

8. The chip package in claim **1** further comprising multiple solder bumps, configured for external connection, aligned with said first surface of said die-surrounding layer.

9. The chip package in claim **1** further comprising multiple gold bumps, configured for external coupling being aligned with said first surface of said die-surrounding layer.

10. The chip package in claim **1**, wherein said substrate comprises a silicon substrate.

11. The chip package in claim **1**, wherein said die-surrounding layer comprises epoxy.

12. A chip package comprising:

a substrate having a surface;

a die-surrounding layer directly on said surface of said substrate;

a die having a backside surface directly on said surface of said substrate, said die disposed between a first portion of said die-surrounding layer and a second portion of said die-surrounding layer, wherein said die has an active surface substantially coplanar with a first surface of said die-surrounding layer, wherein said die comprises a first conductive pad and a second conductive pad within said active surface;

a first dielectric layer on said active surface of said die and on said first surface of said die-surrounding layer; and

a patterned conductive layer on said first dielectric layer, on said active surface of said die and on said first surface of said die-surrounding layer, wherein said patterned conductive layer is coupled to said first conductive pad of said die through a first opening in said first dielectric layer, and wherein said patterned conductive layer is coupled to said second conductive pad of said die through a second opening in said first dielectric layer, wherein said first conductive pad is coupled to said second conductive pad through said patterned conductive layer, wherein said patterned conductive layer comprises a portion of a passive device formed in said patterned conductive layer in a single horizontal plane and a portion configured for external coupling of said die.

13. The chip package in claim **12**, wherein said die-surrounding layer comprises epoxy.

14. The chip package in claim **12** further comprising multiple solder bumps, configured for external connection, vertically over said first surface of said die-surrounding layer.

15. The chip package in claim **12**, wherein said first dielectric layer comprises polyimide.

16. The chip package in claim **12**, wherein said first dielectric layer comprises benzocyclobutene (BCB).

17. The chip package in claim **12** further comprising a second dielectric layer on said patterned conductive layer and on said first dielectric layer.

18. The chip package in claim **17**, wherein said second dielectric layer comprises polyimide.

19. The chip package in claim **17**, wherein said second dielectric layer comprises benzocyclobutene (BCB).

20. The chip package in claim **12**, wherein said patterned conductive layer comprises a ground bus coupling said first conductive pad to said second conductive pad.

21. The chip package in claim **12**, wherein said patterned conductive layer comprises a power bus coupling said first conductive pad to said second conductive pad.

22. The chip package in claim **12**, wherein said patterned conductive layer comprises a signal trace coupling said first conductive pad to said second conductive pad.

23. The chip package in claim **12**, wherein said passive device comprises a micro electro mechanical sensor.

24. The chip package in claim 12, wherein said passive device comprises an inductor.

25. The chip package in claim 12, wherein said passive device comprises a capacitor.

26. The chip package in claim 12, wherein said passive device comprises a resistor.

27. The chip package in claim 1, wherein said substrate comprises a silicon substrate.

28. The chip package in claim 12, wherein said portion of said passive device is aligned with said first portion of said die-surrounding layer.

29. A chip package comprising:

a substrate having a surface;

a die-surrounding layer directly on said surface of said substrate;

a die having a backside surface directly on said surface of said substrate, said die disposed between a first portion of said die-surrounding layer and a second portion of said die-surrounding layer, wherein said die has an active surface substantially coplanar with a first surface of said die-surrounding layer, wherein said die comprises a first conductive pad and a second conductive pad within said active surface;

a first dielectric layer on said active surface of said die and on said first surface of said die-surrounding layer; and

a patterned conductive layer on said first dielectric layer, on said active surface of said die and on said first surface of said die-surrounding layer, wherein said patterned conductive layer comprises a ground piece coupled to said first conductive pad of said die through a first opening in said first dielectric layer, and coupled to said second conductive pad of said die through a second opening in said first dielectric layer, wherein said first conductive pad is coupled to said second conductive pad through said ground piece, wherein said patterned conductive layer comprises a portion of a passive device formed in said patterned conductive layer and a portion configured for external coupling of said die.

30. The chip package in claim 29, wherein said passive device comprises an inductor.

31. The chip package in claim 29, wherein said passive device comprises a resistor.

32. The chip package in claim 29, wherein said die-surrounding layer comprises epoxy.

33. The chip package in claim 29, wherein said passive device comprises a capacitor.

34. The chip package in claim 29, wherein said first dielectric layer comprises polyimide.

35. The chip package in claim 29 further comprising a second dielectric layer on said patterned conductive layer and said first dielectric layer.

36. The chip package in claim 29, wherein said first dielectric layer comprises benzocyclobutene (BCB).

37. The chip package in claim 29 further comprising multiple solder bumps, configured for external coupling aligned with said first surface of said die-surrounding layer.

38. The chip package in claim 29 further comprising a substrate supporting said die and said first and second portions of said die-surrounding layer.

39. The chip package in claim 29, wherein said substrate comprises a silicon substrate.

40. The chip package in claim 29, wherein said passive device comprises a micro electro mechanical sensor.

41. The chip package in claim 29, wherein said patterned conductive layer comprises electroplated copper.

42. The chip package in claim 12, wherein said patterned conductive layer comprises electroplated copper.

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